CLAIMS:

What is claimed is:

1. A semiconductor assembly comprising:
   a semiconductor wafer having a plurality of integrated circuits, each circuit having a plurality of metal contact pads as electrical entry and exit ports;
   an electrically conductive array, substantially parallel to the surface of said wafer, comprising a multitude of coupling members positioned so that at least one of said coupling members is electrically in contact with one circuit contact pad, respectively, while remaining insulated from its adjacent coupling member;
   an interposer of electrically insulating material having electrically conductive paths extending through said interposer from one surface to the opposite surface, forming electrical entry and exit ports on said insulating interposer;
   said interposer positioned substantially parallel to the wafer surface and having one of its surfaces attached to said planar array, thereby electrically connecting said ports to at least some of said coupling members; and
   a planar array of solder balls attached to said exit ports of said interposer.
2. The semiconductor assembly of Claim 1 wherein said semiconductor wafer comprises silicon, gallium arsenide or any other semiconductor material used in electronic device production.
3. The semiconductor wafer of Claim 2 wherein said metal contact pads of said semiconductor wafer comprise aluminum, copper, a refractory metal, a noble metal, or layers thereof.
4. The semiconductor wafer of Claim 3 wherein said refractory metal comprises chromium, molybdenum, titanium, tungsten, or alloys of each.
5. The semiconductor wafer of Claim 3 wherein said noble metal comprises palladium, gold, platinum, silver, or alloys thereof.
6. The semiconductor assembly of Claim 1 wherein said coupling members comprise discrete solder balls.
7. The semiconductor assembly of Claim 6 wherein the space between said discrete solder balls is ambient or filled with epoxy or other electrically insulating plastic material.
8. The semiconductor assembly of Claim 1 wherein said coupling members comprise a multitude of electrically conductive fibers extending through an electrically nonconductive layer from one surface to the opposite surface, while remaining insulated from adjacent fibers.
9. The semiconductor assembly of Claim 1 wherein said electrically insulating interposer is mechanically elastic.
10. The semiconductor assembly of Claim 9 wherein said mechanically elastic interposer comprises polyimide, epoxy, resin, and/or reinforcing material.

11. The semiconductor assembly of Claim 1 wherein said electrically insulating interposer comprises ceramic material.

12. The semiconductor assembly of Claim 1 wherein said electrically conductive paths comprise gold or copper when said electrically insulating interposer is organic material, and comprise tungsten or tungsten alloy when said insulating interposer is ceramic.

13. The semiconductor assembly of Claim 1 wherein said electrical entry and exit ports of said electrically insulating interposer comprise copper or tungsten arrays overlaid by palladium, gold, platinum, or platinum-rich alloy.

14. A method for the fabrication of a semiconductor assembly comprising:

providing a semiconductor wafer having a plurality of integrated circuits, each circuit having a plarality of metal contact pads as electrical entry and exit ports;

forming a planar array of solder balls attached to said contact pads of said semiconductor wafer so that each of said contact pads is contacted by one of said solder balls;

providing an interposer of electrically insulating material having electrically conductive paths from one surface to the opposite surface, forming electrical entry and exit ports on said insulating interposer;

aligning said interposer with said solder balls so that each port is placed into alignment with one of said solder balls on said semiconductor wafer;

contacting said ports and said solder balls;

applying energy to said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing the solder balls to reach a liquid state;

removing said energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said ports; and

separating the resulting composite structure into discrete chips.

15. A method for the fabrication of a semiconductor assembly comprising:

providing a semiconductor wafer having a plurality of integrated circuits, each circuit having a plurality of metal contact pads as electrical entry and exit ports;

forming a first planar array of solder balls attached to said contact pads of said semiconductor wafer so that each of said contact pads is contacted by one of said solder balls; .

providing an interposer of electrically insulating material having electrically conductive paths from one surface to the opposite surface, forming electrical entry and exit ports on said insulating interposer;

aligning said interposer with said solder balls so that each port is placed into alignment with one of said solder balls on said semiconductor wafer;

contacting said ports and said solder balls;

applying energy to said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing said solder balls to reach a liquid state;

removing said energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said ports;

forming a second planar array of solder balls attached to said exit ports of said interposer so that each of said exit ports is contacted by one of said solder balls; and

separating the resulting composite structure into discrete chips.

16. A method for the fabrication of a semiconductor assembly comprising:

providing a semiconductor wafer having a plurality of integrated circuits, each circuit having a plurality of metal contact pads as electrical entry and exit ports;

providing an adhesive layer having a multitude of electrically conductive fibers extending through electrically nonconductive material from one surface to the opposite surface of the layer while remaining insulated from adjacent fibers;

providing an interposer of electrically insulating material having electrically conductive paths from one surface to the opposite surface, forming electrical entry and exit ports on said insulating interposer;

placing said interposer vertically and in contact with said adhesive substrate;

providing a polymer film having a plurality of discrete adhesive areas;

providing a plurality of solder balls, one of said solder balls being placed on each of said adhesive areas;

aligning said polymer film to said interposer so that each of said solder balls is placed into alignment with one of said ports;

placing said solder balls in contact with said ports;

applying energy to said semiconductor wafer such that said wafer uniformly increases in temperature and transfer heat to said adhesive substrate, said interposer and said solder balls, causing said solder balls to reach a liquid state;

removing said energy such that all said contacts form physical bonds and said solder balls cool and harden, forming physical bonds between said solder balls and said ports;

removing said polymer film; and

separating the resulting composite structure into discrete chips.

17. The method according to Claim 14, Claim 15, and Claim 16 wherein said solder balls comprise at least one alloy with a melting temperature compatible with multiple reflow.

18. The method according to Claim 14, Claim 15, and Claim 16, wherein said wafer contact pads, said solder balls, and said interposer ports comprise a combination of materials such that metal interdiffusion is minimized.